Options:_____

Date Received:_____

Software Revision:_____

AEC-BOX-80/81/82/83
VTR SERIAL CONTROL ADAPTERS
INSTRUCTION MANUAL

ADRIENNE ELECTRONICS
CORPORATION

AEC-BOX-80: Serial Adapter for Parallel Remote VTR's
(control only - no time code capabilities)

AEC-BOX-81: Serial Adapter with LTC Reader
AEC-BOX-81G: Serial Adapter with LTC Reader/Generator

AEC-BOX-82: Serial Adapter with VITC Reader
AEC-BOX-82G: Serial Adapter with VITC Reader/Generator

AEC-BOX-83: Serial Adapter with LTC/VITC Reader
AEC-BOX-83G: Serial Adapter with LTC/VITC Reader/Generator

VTR Type: _____

Fourth Edition January 1997

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*** FCC NOTICE ***

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, could cause harmful interference to radio communications. Operation of this equipment in a residential area may cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

*** COPYRIGHT NOTICE ***

Also, due to copyright restrictions, we cannot provide you with a detailed description of the "Sony" serial protocol. We suggest that you contact them about ordering a copy if needed.

*** TRADEMARK NOTICES ***

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INTRODUCTION

Adrienne Electronics Corporation (AEC) developed the AEC-BOX-80 series of Serial Adapters for Parallel Remote VTR's in order to provide a low cost way of controlling such VTR's using a variety of personal computers and other devices. The optional LTC/VITC reader and generator functions provide time code capabilities not previously available to parallel remote VTR's. Thus, when connected to an AEC-BOX-80, parallel remote VTR's can be used in place of more modern (and more expensive) serial remote VTR's.

Two different serial protocols are supported by each AEC-BOX-80. A simple DIP switch change selects whether to use the Sony or AEC protocol. The "Sony" protocol (38400 baud, 8 data bits, and ODD parity) is the same as that used on Betacam and U-matic broadcast quality VTR's. The "AEC" protocol (9600 baud, 8 data bits, and no parity) is one we have devised which has more features and is much easier to use with personal computers.

These boxes work equally well with SMPTE (30fps) and EBU (25fps) time codes, in both the forward and reverse tape directions.

NOMENCLATURE

The term "AEC-BOX-80" will be used in this manual to refer to all members of the AEC-BOX-80/81/82/83 family. Where not obvious, differences in behavior between the various boxes will be pointed out. In addition, the word "CONTROLLER" will be used to refer to whatever device is sending commands to the "AEC-BOX-80".

GETTING STARTED QUICKLY

If you want to use your AEC-BOX-80 right away, without reading the whole manual, just do the following:

1) Make sure the power to your VTR is OFF!
2) Connect the parallel control cable to the VTR and AEC-BOX-80.
3) Turn ON your VTR. The box LED should blink several times.
4) Use a serial data cable to connect the AEC-BOX-80's 9-pin "SERIAL CONTROL" connector to your computer or other device.
5) Connect "LTC OUT" on your VTR to "LTC IN" on the AEC-BOX-80, "VIDEO OUT" on your VTR to "VITC IN" on the AEC-BOX-80, etc..

If something doesn't work, you will have to carefully read the "INSTALLATION" section of this manual.

AEC-BOX-80 SPECIFICATIONS

LTC READER:	
Input Impedance	10kohms typical
Input Level	100mVpp to 20Vpp
DC on Input	+1V maximum
Speed Range (2)	1/30x to 50x (w.r.t. play speed)
Tape Direction	Forward or Reverse
Bits Read	ALL time, user, and embedded bits.
Time Code Standard	Both SMPTE and EBU, without modification.
VITC READER (AND VIDEO SYNC INPUT):	
Impedance	6kohms typical (Hi-Z)
Input Level	0.8Vpp to 2.2Vpp (1Vpp nominal)
Looping Response	+0.1db maximum, 0-5MHz
Video Frequency	Must be within 5% of nominal frequency.
Speed Range (3)	-1x to STILL to +3x (w.r.t. play speed)
Tape Direction	Forward or Reverse
Bits Read	ALL time, user, and embedded bits.
Time Code Standard	SMPTE/EBU selected by switch or software
LTC GENERATOR:	
Output Level	1Vpp typical
Output Impedance	100ohms typical
Bits Written	ALL time, user, and embedded bits.
Time Code Standard	SMPTE/EBU selected by switch or software.
VITC ADDER:	
Pulse Shapes	Comply with SMPTE/EBU specifications.
Looping Response	+0.1db maximum, 0-5MHz
Video Frequency	Must be within 1% of nominal frequency.
Bits Written	ALL time, user, and embedded bits.
Line Selection	Determined by software.
Time Code Standard	SMPTE/EBU selected by switch or software.
MISCELLANEOUS:	
Box Dimensions (4)	16cm wide x 5cm high x 21cm long
Box Weight	0.7kg
Power Consumption	6W
Temperature Range	0 to 50 degrees Centigrade
Relative Humidity	Up to 95%, noncondensing

Notes:
(1) All specifications are subject to change without notice.
(2) LTC signals below play speed are often too distorted to read.
    Varies with tape format, tape machine, etc.
(3) Highly VTR dependent. Some are better, some are worse.
(4) Allow at least 6cm on each end for cables and connectors.

Throughout the following discussion you may want to refer to the AEC-BOX-80 schematics which are in the back of this manual. If your box has been customized in any way for your application, or if your box does not have all of the possible features installed, then the descriptions below may not be entirely accurate.

Operating power for the AEC-BOX-80 is obtained from the VTR via the parallel control cable. This supply voltage is then converted to +5V (for internal use) by voltage regulator U21.

If the LTC reader option is installed, RCA jack J4 provides the input connection. An LTC input signal is first AC coupled by C25, then is fed into the window comparator comprising quad comparator U11 and surrounding components. This comparator automatically senses the incoming signal level and adjusts itself as needed to recover the LTC transition data even from very poor quality input signals. The complementary outputs of the window comparator go directly to proprietary LTC reader chip U9.

If the LTC generator option is installed, microcomputer (U7) pin 7 drives Q2 on and off as needed to create the desired biphase coded data pattern. RN9A and C30 create the required sloped edges, and D12 and D13 limit the amplitude. Buffer transistors Q4 and Q3 drive the output via AC coupling capacitor C27. RCA jack J5 provides the output connection.

The video sync input is only taken from the two "VITC ADD" BNC's when the VITC generator is present and active. Otherwise the video sync input is taken from the two "SYNC/VITC IN" BNC's. When the VITC generator option is installed, relay K1 (driven by Q9 and U8 pin 25) automatically selects the proper sync source. Video signals may be looped through the AEC-BOX-80 with negligible losses, as the BNC's are wired directly to each other.

The video sync (which may contain VITC) input signal is DC shifted by C39, then passes through 3-pole low pass filter R15, C38, L1, and C37, with buffer Q7. Transistor Q6 is turned on by each negative sync tip, and thus generates horizontal sync pulses which are fed to U7 pin 1. Low pass filter RN11D, R12, and C36 only allow Q5's collector to go low during vertical reset pulses.

If the VITC reader is installed, OTA U13 is strobed ON during the back porch of each video line, and thus maintains the DC level of the low pass filtered video signal at about +2.5VDC. Comparator U12B generates a voltage equal to the -40IRE (sync tip) level on storage capacitor C31. Comparator U12A compares the VITC input pulses with the +40IRE level, and its digital logic output then goes to pin 16 of proprietary VITC reader chip U8.

If the VITC adder (generator) option is installed, pin 26 of proprietary VITC chip U8 directs current pulses to the "VITC ADD" output BNC's via current switch Q10, Q11. Assuming that the video signal being looped through these BNC's is properly terminated, and assuming that the vertical interval lines are previously "blank", a well shaped VITC signal will then be added to the desired vertical interval lines of the video signal.

Microcomputer U7, together with address latch U3 and EPROM U5, form a completely self contained (but miniature) computer system. A "watch dog" timer inside the microcomputer chip resets everything if the software crashes for some reason. The low voltage detection circuit centered about Q14 also resets the microcomputer during power up, power down, and low supply voltage ("brownout") conditions.

Connector J2 contains 37 pins which may be used to control the VTR and to sense the VTR's status. There are 18 dedicated output pins, 10 dedicated input pins, and 6 bi-directional I/O pins. Octal latches U4, U17, and U19 drive the output pins via buffer transistors Q18-Q42, which also invert the signal polarity. Octal buffers U18 and U20 can be read by the microcomputer to sense the polarity of the input lines.

DIP switch SW1 allows easy modification of box operating modes and features. The green "power" LED is driven by Q17 and microcomputer pin 5 to indicate the current box status. Serial EEPROM U6 stores various setup and VTR characteristics information even when the power is off. This allows the AEC-BOX-80 to adapt and optimize itself for the VTR being used.

Serial data from UART U15 is translated to RS232 levels by U2, and is translated to RS422 levels by U1. U1 also translates received RS232 and RS422 data for use by UART U15. Nine pin "D" connector J1 contains the RS232 and RS422 transmit and receive data lines.

AEC-BOX-80 EXTERNAL CABLING INSTALLATION

LTC INPUT CONNECTION:
If the LTC reader option is installed, RCA jack J4 is the high impedance (10kohm) LTC input connector. Typically it should be connected to the "TIME CODE OUTPUT" jack on the back of the VTR. Note that J4's outer conductor is connected to frame ground (the box chassis).

LTC OUTPUT CONNECTION:
If the LTC generator option is installed, RCA jack J5 is the low impedance (100ohm) LTC output connector. Typically it should be connected to the "TIME CODE INPUT" jack on the back of the VTR. Note that J5's outer conductor is connected to frame ground (the box chassis).

VITC INPUT CONNECTION:
If the VITC reader option is installed, you should loop the cable coming from the VTR's "VIDEO OUTPUT" connector through the two "SYNC/VITC IN" BNC connectors on the AEC-BOX-80. These two connectors are wired together, and have negligible effect on the video signal (see specifications). For best frequency response and VITC readability, be sure to properly terminate the video cable with 75ohms either at the AEC-BOX-80 or at the far end of the cable. The nominal video input level is 1Vpp, but the input amplifiers will adjust themselves to other input levels, including the unterminated cable condition.

VITC OUTPUT CONNECTION:
If the VITC adder (generator) option is installed, you should first loop the cable going to the VTR's "VIDEO INPUT" connector through the two "VITC ADD" BNC connectors on the AEC-BOX-80. These two connectors are wired together, and have negligible effect on the video signal (see specifications). It is always assumed that the looping video signal level is 1Vpp, and that the video cable is properly terminated with 75ohms both at the video source and at the VTR (which may have an internal termination).

PARALLEL VTR CONTROL CABLE:
First make absolutely sure that the power to the VTR is OFF! Then connect the "PARALLEL REMOTE" connector on the back of the VTR to the 37-pin "D" parallel interface connector on the AEC-BOX-80, using the cable supplied. The VTR can then be turned on.

SERIAL INPUT/OUTPUT CONNECTIONS:
If you ordered a serial data cable with your AEC-BOX-80, just plug the appropriate end into the standard 9-pin "D" subminiature "SERIAL CONTROL" connector on the box. Otherwise, you may use the kit of mating connector parts to wire up to the box as follows:

Pin #	Function
1	GND
2	TX422-
3	RX422+
4	
5	TX232
6	
7	TX422+
8	RX422- and RX232
9	GND

Notes:
1) Tiny pin numbers are molded into the connector face.
   Be careful not to be "off by one".
2) For RS422, note that the pinout is that of an ESbus Tributary.
3) Limit RS232 cables to 30 meters maximum.
4) Limit RS422 cables to 1200 meters maximum.
5) The AEC-BOX-80 connector has socket type contacts, so your
   cable should have pin type contacts.
6) AEC-BOX-80 transmit lines should be connected to the
   controller's receive lines, and vice-versa.

DIP SWITCH PROGRAMMING

Box Cover Removal:
First you must turn off power to the box and remove all external cables. Then you may remove the top cover as follows:

1) Use a small (#1) Phillips screwdriver to remove the two small black screws which are on each side of the box.
2) Slide off the front and back black plastic bezels.
3) Lift off the top cover.

Changing DIP Switch (SW1) Settings:
Note that the switches are numbered 1 through 8. Also note the small "1" and "0" numbers which are on the left and right ends of SW1. To set a switch to be a "1", simply press down on the "1" (OPEN) end of that switch. Conversely, to set a switch to be a "0", simply press down on the "0" end of that switch. All done!

DIP Switch Functionality:

Switch	Function
8	Sony(1) or AEC(0) Serial Interface Protocol
7	Diagnostics(1) or Normal(0) Operations (see page 28)
6	reserved
5	reserved
4	reserved
3	reserved
2	reserved
1	reserved

Factory Default Setting:
Unless you requested otherwise, the factory default setting is AEC serial interface protocol (9600 baud, 8 bits, no parity), so SW1 will normally be 00000000 for switches 1-8, respectively.

Box Cover Replacement:
Basically, just follow the earlier instructions in reverse order:

1) Put the top cover back in place.
2) Slide a black plastic bezel onto each end of the unit. The box looks better if the two small molding marks are facing towards the bottom of the unit.
3) Reattach the bezels to the chassis with the four small black screws you removed earlier. Be careful not to strip the threads in the aluminum side extrusions!
4) Reattach all cables, then turn on the power.

LTC READER OPERATIONS

This section only applies if the LTC reader option is installed.

A proprietary chip is used to read the LTC input signal present at the "LTC IN" RCA jack. The reader will properly read both SMPTE and EBU LTC signals in both the forward and reverse directions, with LTC input signal levels ranging from 100mVpp to 20Vpp, and at tape speeds from 1/30x to 50x play speed.

If the LTC input signal is severely distorted, as is often the case when tape machines are played back at speeds below 1/2x, the reader may not be able to decode the LTC signal without errors. The lowest useable speed is highly dependent on the tape and tape machine that you are using, so you'll just have to use trial and error to find out what the minimum useable speed is. Even a single bit error out of the 80 in each LTC frame is enough to invalidate the entire frame.

In the case where LTC read errors are detected, the AEC-BOX-80 will either use VITC data instead (if valid), or it will use control track pulses from the VTR to adjust the last valid LTC count up or down (by one count per control track pulse).

VITC READER OPERATIONS

This section only applies if the VITC reader option is installed.

A proprietary chip is used to read VITC from the video signal present at the "SYNC/VITC IN" BNC's. The reader will properly read both NTSC/SMPTE and PAL/EBU VITC signals in the STILL (PAUSE) mode, and with tape speeds up to +10 times play speed on some VTR's. The VITC reader also filters out noise, and includes automatic level sensing circuits to compensate for input levels other than the nominal 1Vpp.

The VITC signal is usually present on two nonadjacent lines (for redundancy) in each vertical interval. Lines 10-20 are normally used with NTSC, and lines 6-22 are normally used with PAL. The box needs to be in the SMPTE/NTSC mode to read VITC from NTSC video signals, and needs to be in the EBU/PAL mode to read VITC from PAL video signals. The box mode may be changed via the BOXSETUP program (on the diskette) if needed.

The VITC reader needs to know which lines have VITC on them. When the power is first turned on (or if the box resets itself) the box reads the line numbers which have been stored in the EEPROM. You can change these EEPROM values by using the BOXSETUP program (on the diskette) if needed.

The factory default setting of "0" for both lines tells the VITC reader to read the first two lines which it thinks have VITC on them. If other signals are present in the vertical interval, such as teletext or a second set of VITC lines, it may get confused. Alternatively, you can specify which line numbers to use, as mentioned above. For NTSC, lines 10-25 are accepted. For PAL, lines 6-25 are accepted. The second line number should always be greater than or equal to the first line number. The box will force the numbers to be valid if you choose something which it can't understand.

If a nonstandard vertical sync pulse is detected, which is often the case with non-broadcast type VTR's at anything other than play speed, the VITC reader is unable to count video lines. In this case, the VITC reader will read the first two lines it finds (if any) which have VITC on them, regardless of EEPROM settings.

It is also important to note that those VTR's which generate nonstandard vertical sync pulses often obliterate whatever is on NTSC lines 10-12. PAL machines undoubtedly do similar things. Thus if you are using these type VTR's, and if you have a choice, it is best to place VITC on some of the higher numbered lines.

VITC READER OPERATIONS
(continued)

It has been our experience that VITC is being used more and more often with VHS and other "consumer" quality tape formats. These VTR's often do not have very good frequency and phase response. Since VITC requires accurate reproduction of the first 2MHz of the video signal, use of VITC on these machines is often marginal. Sometimes they will work pretty well at play speed, but not much else. Poor quality VITC waveforms simply cannot be read.

When working at other than play speed, the tape speeds at which VITC can be read are highly machine dependent. With some tape machines we have been able to read VITC at up to +10 times play speed. Other tape machines destroy or distort the VITC waveforms at some speeds, yet work fine at both higher and lower speeds. Experimentation on your part is usually in order. We'd like to hear about your findings.

The VITC reader always uses the data read from the first VITC line, if it is OK. Otherwise it will use the data read from the second VITC line, if that is OK. If both lines are bad, the AEC-BOX-80 will either use LTC data instead (if valid), or it will use control track pulses from the VTR to adjust the last valid VITC count up or down (by one count per control track pulse).

Read errors are a fact of life, even with good tape machines. The CRC byte in each VITC word provides fairly good error detection capability, but does not eliminate 100% of bad data. You may want to do a few checks on the VITC time data presented to see if it agrees somewhat with previous frame numbers, etc.. We have included a "nonsequential VITC data filter" which ignores a VITC data word if it is more than 10 frame counts off from the current box time. However, if the very next VITC data is also outside this 10 frame window, it will be accepted so that the box will work properly when VITC data first appears, or when it jumps to a new set of values. The VITC data filter can be disabled, if needed, via software command 53h.

Finally, note that VITC data is normally updated every FIELD, whereas LTC data is normally updated only every FRAME. Thus, when reading VITC, the user bits and embedded bits may change twice as often as you may be used to with LTC.

LTC GENERATOR OPERATIONS

This section only applies if the LTC generator option is installed.

Whenever the generator is started, the LTC output signal will appear at the "LTC OUT" jack (J5). When the generator is not running, this output is silent (no signal).

If a video sync input is present, the LTC output will automatically be properly synchronized with it. Otherwise, the LTC output will slowly drift with respect to the video frames on the tape.

Note that putting the VTR into record mode (or doing edits) does not start the generator. Be sure to start the generator(s) BEFORE you start recording or editing.

When you are finished recording or editing, be sure to remember to reenable the LTC and/or VITC time code readers!

VITC GENERATOR OPERATIONS

This section only applies if the VITC generator option is installed.

Whenever the generator is started, the VITC signal will be added to the video signal which is present at the "VITC ADD" connectors. When the generator is not running, the video signal passes through the AEC-BOX-80 unchanged.

By definition, the VITC generator output is always perfectly synchronized with the video signal it is being added to, so there are no possible drift problems as there are with LTC.

Note that putting the VTR into record mode (or doing edits) does not start the generator. Be sure to start the generator(s) BEFORE you start recording or editing.

When you are finished recording or editing, be sure to remember to reenable the LTC and/or VITC time code readers!

COMPARATOR OPERATIONS

This section only applies if you are using the "AEC" protocol.

The AEC-BOX-80 contains comparator software, which allows you to have the box transmit a short message whenever the LTC or VITC time bits (or user bits) (or control track time bits) reach a predetermined value. This frees up your system for other tasks.

Assuming that the comparator is enabled, whenever the time bits are updated, they (or the user bits) are first compared, then masked, with values which you have set up ahead of time. If a match is detected (after masking), a bit will be set which may be sensed by polling the box. Also, if enabled, an ASCII "=" character (3Dh) will be transmitted when the match occurs.

If the "edge match" bit of the comparator mode control byte is a 1, a "comparison" will be indicated both when the match first occurs, and again when the match disappears. It detects the "edges", and avoids generating lots of comparison indications when successive frames have the same data (after masking).

If you are using SMPTE drop frame counting, be sure not to set up a comparison time, such as 00:01:00:00, which doesn't exist.

The comparator data and mask bytes may be changed at any time. See page 20 of the software protocol section for details.

The comparator mode is changed by command 54h (page 19), and the comparator status may be sensed by command D4h (page 23). The power on default is to have the comparator disabled.

HOW TO USE COMPARATOR MASKS

There are many cases where you don't care what the value of one or more bits is, but you still want to use the comparator. To do this, just set the corresponding mask bit(s) to zero. For instance, if you want the box to transmit an "=" character every ten seconds, set the seconds mask byte to 0Fh, and set the minutes and hours mask bytes to 00h.

The comparator first does a logical XOR (comparison) of the current time (or user) data with the data you have supplied ahead of time. It then does a logical AND of the results with the mask data you have supplied. In positions where the mask data is 0, a "match" is always indicated. In positions where the mask data is 1, an exact match is required.

The default masks of 3Fh (for hours and frames) and 7Fh (for minutes and seconds) are used to filter out six special bits, called embedded bits, which are usually mixed in with the time bits. Always mask them out when not being used!

"AEC" PROTOCOL DESCRIPTION

Adrienne Electronics Corporation (AEC) developed this protocol (9600 baud, 8 data bits, no parity) in order to make it easy to control VTR's with a variety of personal computers and other devices. Special attention has been paid to supporting time code functions. We also made it easy to use with popular BASIC, C, Pascal, and Assembly language compilers, assemblers, and interpreters.

We chose 9600 baud because it is the highest rate which is widely supported by personal computer hardware and software. Eight data bits were required for sending time code data efficiently. The use of NO parity is required by many PC's and compilers when eight data bits are used. Even though no parity is used, the message protocol outlined below provides excellent serial data error detection capabilities.

The command protocol has been chosen to minimize the number of serial data characters which must be sent. For example, most VTR transport commands, such as STOP, PLAY, PAUSE, and REWIND, are only one byte long! This dramatically speeds up system performance.

For your convenience, time code input and output data may be in either the standard packed BCD format (HH:MM:SS:FF) or in a special binary (0-2591999 for SMPTE) format. The binary format allows easy calculation of event durations and easy program storage of time code numbers.

GENERAL PROTOCOL NOTES:

1) The AEC-BOX-80 should respond within 10ms to all commands. If it fails to do so, or if it returns the wrong data, a failure of some kind is indicated.
2) Sending command codes other than those listed in this protocol description will lead to unpredictable results.
3) Be careful not to send a carriage return (0Dh) or line feed (0Ah) after any commands! Some compilers, such as BASIC, send these characters automatically unless you disable them.
4) Whenever multiple byte messages are sent to the AEC-BOX-80, it expects there to be no more than a 10ms delay between received bytes. Otherwise the box flags a timeout error and ignores the message.
5) When the box first powers up, when it gets reset, and when it detects communications errors, it will ignore all received data until it sees a 12ms or longer gap between bytes from the controller. This ensures that the box and controller are properly synchronized.
6) Reception of a reply from the AEC-BOX-80 does not necessarily mean that the operation is complete. This is especially true for searches and other VTR transport control functions. Your software should request status messages to determine when the VTR and AEC-BOX-80 are ready for the next operation.

TIME CODE INTERFACE NOTES:

1) There is only one "time" inside the AEC-BOX-80, which is stored in packed BCD format. VTR control pulses are used to adjust this time up and down in the absence of LTC/VITC time code inputs.
2) When the box first powers up, and when it is reset, the internal "time" defaults to 00:00:00:00. If VITC and/or LTC readers are being used, your software should first PLAY the tape until at least one frame of time code has been read. Otherwise the first search operation will not know where it is on the tape, and will probably not work correctly.
3) For all box operations, it is always assumed that all time codes are sequential and within 11 hours of each other. This restriction allows a search from 00:01:00:00 to 23:59:00:00 to proceed in the REVERSE direction, as it should.
4) If time code is nonsequential, time code search commands will get confused. This problem can be avoided by disabling the LTC/VITC readers during searches (if necessary), so that only control pulses are used for the search process.
5) Whenever packed BCD time code information is sent, the HOURS byte is always sent first, followed by the MINUTES, then the SECONDS, and lastly the FRAMES.
6) Whenever binary time code information is sent, the LEAST SIGNIFICANT byte is always sent first. Subsequent bytes have increasing significance. The last byte should always be 00h. This format allows direct (easy) conversion to and from BASIC long integers, as are found in Microsoft QuickBASIC 4.0+.
7) After any reset, the box assumes that packed BCD time code I/O will be used. Command B1h can be used to specify binary time code I/O. The I/O mode can be changed at any time, since it only affects the I/O format and does not change any internal time code numbers (which are always packed BCD). For example, you may want to use binary I/O for time bits, and packed BCD I/O for user bits.
8) To avoid confusion, especially if the AEC-BOX-80 could get reset in the middle of your program, you may want to preface all time code I/O commands/requests with command B0h or B1h (as appropriate).
9) The six special embedded bits are never present in any time bits I/O. They are instead set and read by other commands. See the commands list for details.

MISCELLANEOUS NOTES:

1) Unless noted otherwise, whenever the box is reset, all bytes default to 00h and all bits default to "0".
2) For your convenience, all command codes are shown in both decimal(d) and hexadecimal(h) formats.

TWO BYTE MESSAGES:
These messages are used primarily for sending setup information to the AEC-BOX-80. Each two byte message consists of a command byte followed by one data byte.

When the controller sends one of these messages to the AEC-BOX-80, the AEC-BOX-80 will echo the same two bytes back to the controller. This is done for error detection purposes. If the box does not return anything within 10ms, or if it returns the wrong bytes, a failure is indicated. The controller may ignore the returned bytes if desired (for simplicity), but we do not recommend this approach for any commercial or other critical applications.

The data byte formats, where not obvious, are explained below. Following are the command byte codes:

064d/40h => Shuttle Forward at the speed indicated.
065d/41h => Shuttle Reverse at the speed indicated.
Speed = 10**(data/32d - 2):

Speed	Decimal Code	Hex Code
10x	96d	60h
6x	89d	59h
5x	86d	56h
2x	74d	4Ah
1x	64d	40h
1/2x	54d	36h
1/5x	42d	2Ah
1/10x	32d	20h
1/25x	19d	13h

Note that speeds available are VTR dependent.

080d/50h => Set AEC-BOX-80 Embedded Bits:
Bit 5 => LTC bit 59
Bit 4 => LTC bit 58
Bit 3 => LTC bit 43
Bit 2 => LTC bit 27
Bit 1 => LTC bit 11
Bit 0 => LTC bit 10 (drop frame flag)

081d/51h => Do software reset if the data byte is also 51h.

082d/52h => Set time code enables (default is 13h):
Bit 4 => Enable control pulse reader.
Bit 3 => Enable VITC generator.
Bit 2 => Enable LTC generator.
Bit 1 => Enable VITC reader.
Bit 0 => Enable LTC reader.

TWO BYTE MESSAGES:
(continued)

083d/53h => Set time code mode:
Bit 5 => Disable nonsequential VITC data filter.

084d/54h => Set comparator mode (default is 01h):
Bit 7 => reserved
Bit 6 => reserved
Bit 5 => reserved
Bit 4 => reserved
Bit 3 => Enable "edge" comparisons (see text).
Bit 2 => Transmit "=" when comparator triggers.
Bit 1 => Compare user bits instead of time bits.
Bit 0 => Disable all comparator functions.

086d/56h => Set first VITC line number (binary 0-31).
087d/57h => Set second VITC line number (binary 0-31).

088d/58h => Set AEC-BOX-80 mode bits:
Bit 4 = 1 if want PAL/EBU mode

FIVE BYTE MESSAGES:
These messages are used primarily for sending time and user bits information to the AEC-BOX-80. Each five byte message consists of a command byte followed by four data bytes.

When the controller sends one of these messages to the AEC-BOX-80, the AEC-BOX-80 will echo the same five bytes back to the controller. This is done for error detection purposes. If the box does not return anything within 10ms, or if it returns the wrong bytes, a failure is indicated. The controller may ignore the returned bytes if desired (for simplicity), but we do not recommend this approach for any commercial or other critical applications.

The four data bytes are in standard time code format, as described elsewhere. Following are the command byte codes:

096d/60h => Set AEC-BOX-80 Time Bits

098d/62h => Set AEC-BOX-80 User Bits

108d/6Ch => Set Comparator Data Bytes

109d/6Dh => Set Comparator Mask Bytes

112d/70h => Go to the frame indicated, then pause.

SINGLE BYTE MESSAGES:
These messages are used primarily for VTR transport control and for AEC-BOX-80 mode control.

When the controller sends one of these messages to the AEC-BOX-80, the AEC-BOX-80 will echo the same byte back to the controller. This is done for error detection purposes. If the box does not return anything within 10ms, or if it returns the wrong byte, a failure is indicated. The controller may ignore the returned byte if desired (for simplicity), but we do not recommend this approach for any commercial or other critical applications.

Following are the command codes:

128d/80h => Stop (with no tape video output)

129d/81h => Pause (with tape video output)

130d/82h => Play

132d/84h => Fast Forward

133d/85h => Rewind

134d/86h => Step Forward (one frame)

135d/87h => Step Reverse (one frame)

136d/88h => Record (crash record, all channels)

147d/93h => Eject

176d/B0h => Use packed BCD time code I/O (default).

177d/B1h => Use binary time code I/O instead.

SINGLE DATA BYTE REQUEST MESSAGES:
The following command codes are used for requesting one byte of data (usually some kind of status) from the AEC-BOX-80.

When the controller sends one of these command codes to the AEC-BOX-80, the AEC-BOX-80 will return a special code byte back to the controller, followed by the desired data byte, followed by a checksum byte. If the box does not return anything within 10ms, or if it returns anything incorrect, a failure is indicated. The controller may ignore the returned code and checksum bytes if desired (for simplicity), but we do not recommend this approach for any commercial or other critical applications.

The checksum byte returned is chosen by the AEC-BOX-80 so that the 8 bit sum of all three returned bytes should be zero.

Following are the command codes for requesting one data byte, plus a description of the message(s) that will be returned:

193d/C1h => Get VTR status (or BOX error code):
Response is 41h:data:chk.
See page 25 for status codes.

208d/D0h => Read embedded bits:
Response is 50h:data:chk if time code is OK.
Response is 51h:data:chk if time code is bad.
Bit map is the same as for command 50h.

210d/D2h => Read time code enables:
Response is 52h:data:chk.
Bit map is the same as for command 52h.

211d/D3h => Read time code and video status:
Response is 53h:data:chk.
The bit map of this data byte is as follows:
Bit 7 = 1 if the video input is OK
Bit 6 = 1 if reading LTC in Auto LTC/VITC mode
Bit 5 = 1 if nonsequential VITC is not filtered
Bit 1 = 1 if the VITC input is OK
Bit 0 = 1 if the LTC input is OK

SINGLE DATA BYTE REQUEST MESSAGES:
(continued)

212d/D4h => Read comparator mode/status:
Response is 54h:data:chk.
The bit map of this data byte is as follows:
Bit 7 => Comparator has been triggered.
Bit 6 => Comparator currently has a match.
Bit 5 => reserved
Bit 4 => reserved
Bit 3 => "Edge" comparisons are enabled.
Bit 2 => Will transmit "=" when triggered.
Bit 1 => Will compare user bits, not time bits.
Bit 0 => Comparator is disabled.
NOTE - Reading this register clears bit 7.

214d/D6h => Read first VITC line number (0-31).
Response is 56h:data:chk.

215d/D7h => Read second VITC line number (0-31).
Response is 57h:data:chk.

216d/D8h => Read miscellaneous AEC-BOX-80 status bits:
Response is 58h:data:chk.
The bit map of this data byte is as follows:
Bit 7 = 1 if binary time code I/O is selected
Bit 4 = 1 if PAL/EBU mode is selected
Bit 0 = 1 if box is busy "pressing a button"

FOUR DATA BYTE REQUEST MESSAGES:
The following command codes are used for requesting four bytes of data (usually time or user bits information) from the AEC-BOX-80.

When the controller sends one of these command codes to the AEC-BOX-80, the AEC-BOX-80 will return a special code byte back to the controller, followed by four data bytes, followed by a checksum byte. If the box does not return anything within 10ms, or if it returns anything incorrect, a failure is indicated. The controller may ignore the returned code and checksum bytes if desired (for simplicity), but we do not recommend this approach for any commercial or other critical applications.

The checksum byte returned is chosen by the AEC-BOX-80 so that the 8 bit sum of all six returned bytes should be zero.

Following are the command codes for requesting four data bytes, plus a description of the message(s) that will be returned:

224d/E0h => Read AEC-BOX-80 Time Bits:
Response is 60h:HH:MM:SS:FF:chk if time code is OK.
Response is 61h:HH:MM:SS:FF:chk if time code is bad.
If you are using binary time code I/O, the time bits will be in binary (not packed BCD) format.

226d/E2h => Read AEC-BOX-80 User Bits:
Response is 62h:HH:MM:SS:FF:chk if time code is OK.
Response is 63h:HH:MM:SS:FF:chk if time code is bad.
If you are using binary time code I/O, the user bits will be in binary (not packed BCD) format.

236d/ECh => Read Comparator Data Bytes
Response is 6Ch:HH:MM:SS:FF:chk.

237d/EDh => Read Comparator Mask Bytes
Response is 6Dh:HH:MM:SS:FF:chk.

253d/FDh => Read BOX ID Information:
Response is 7Dh:BoxID:VtrID:RevLtr:RevNum:chk.

VTR STATUS (OR BOX ERROR) CODES:
Following are the box error codes (highest priority):
000d/00h => Box was Reset
001d/01h => Parity Error
002d/02h => Framing Error
003d/03h => Break Detected
004d/04h => Overrun Error
005d/05h => Timeout Error
006d/06h => Data Invalid or Out Of Range
007d/07h => Command Not Recognized
(reading any of these codes clears the associated error bit)

Following are the VTR status codes (lower priority):
130d/82h => Stop
134d/86h => Play
135d/87h => Pause
137d/89h => Shuttle
140d/8Ch => Searching
141d/8Dh => Fast Forward
142d/8Eh => Rewind
146d/92h => Ejected (no tape)
147d/93h => Record
150d/96h => Auto Edit
151d/97h => Preview
152d/98h => Review
192d/C0h => other (unknown)

STANDALONE OPERATION

With some special wiring, the AEC-BOX-80 can be used by itself (without a controller) for dubbing and recording purposes. On power-up, if the box detects that pin 1 of the 37-pin "D" connector is being held low, it turns on the time code generator(s), with an initial time code of 00:00:00:00.

In addition, 15 bits of digital information detected on the 37-pin "D" connector are recorded into the user bits field, as shown below, every frame:

Pin #	Bit #	Location	Pin #	Bit #	Location
31	7	UB Seconds	5	7	UB Frames
29	6	UB Seconds	3	6	UB Frames
32	5	UB Seconds	6	5	UB Frames
24	4	UB Seconds	4	4	UB Frames
7	3	UB Seconds	20	3	UB Frames
27	2	UB Seconds	2	2	UB Frames
30	1	UB Seconds	(1)	1	UB Frames
28	0	UB Seconds	21	0	UB Frames

(37DS connector pin 33 is logic GROUND)

Note that input pin 1 must be held low during power-up, and for at least 5 seconds thereafter, in order to enter this special mode of operation. However, once in this mode, pin 1 can be used just like any other digital input, and will be recorded.

Note also that the box must be connected to the VTR during this time, from which it receives its power.

If pin 31 is a logic low, the generator data will be reset to 00:00:00:00. Since this input pin has an internal pull-up resistor, a simple switch closure to ground will provide the required generator data reset pulse.

The "power" LED will flash on and off while in this mode, unless the generator data reset line (pin 31) is being held low. This makes it easy to verify that the generator is running (when flashing) or is being reset (when not flashing).

The digital inputs may be open collector, TTL, CMOS, relay closures, etc., as there are 100kohm pull-up resistors on each input, and the input amplifiers look for TTL signal levels (0.8V maximum for LOW signals, and 2.0V minimum for HIGH signals).

AEC-BOX-80 LED OPERATIONS

The so called "POWER" LED on the front of the box behaves in a variety of ways so that you can have some clues as to what is (or is not) going on inside the box.

When the AEC-BOX-80 is first turned on, a hardware POR (Power On Reset) circuit forces the LED to blink ON for a short (barely noticeable) time. If this POR blink fails to happen, there must be something seriously wrong with the power supply or LED. Check the TROUBLESHOOTING section on page 29 for details.

After the POR blink, there should be at least one or two longer blinks. If the LED remains off, there must be some kind of hardware/software problem. Call us for assistance.

After the POR blink, if the LED blinks twice more, then remains on continuously, you are in the normal (computer controlled) operating mode, and everything is OK.

Thereafter, the LED will blink off for about 500ms if a serial data reception error is detected. These may include setup errors (wrong baud rate, parity, etc.), random communication errors (like parity or framing errors), or protocol errors.

After the POR blink, if the LED blinks only once more, or if it blinks more than twice, you are in the special standalone mode (see page 26), or you may be in the diagnostics mode (page 28).

Note that no matter what mode the box is in, and no matter how many errors are indicated, the LED will always come on at least once per second. This way you will know that the power supply and software are still OK.

AEC-BOX-80 DIAGNOSTICS

At present there is only one diagnostics program, which is activated by setting DIP switch segment 7 to "1" (see page 10).

While in this special diagnostics mode, a 5Ah (ASCII "Z") character will be transmitted out the RS232/RS422 serial port approximately every 10ms, using the selected (Sony or AEC) serial port parameters. You may use an oscilloscope to verify signal levels, and you may test the controller software to make sure that it can receive all the 5Ah characters with no problems.

While in this mode, the "power" LED will flash on and off about once per second. If you short the transmit and receive lines together, either at the box or at the far end of the serial control cable, the LED will flash much more quickly, provided that the AEC-BOX-80 is receiving the same data that it is transmitting. Otherwise there may be a problem with the serial control cable or with the AEC-BOX-80.

The above diagnostic makes it fairly easy to debug the serial interfaces (and cable) between the AEC-BOX-80 and its controller. If you have any ideas for other useful diagnostics programs, please let us know.

AEC-BOX-80 TROUBLESHOOTING GUIDE

This guide lists anticipated problems and their solutions. If you really get stuck, call our Service Department.

Problem #1: Power LED does not blink ON when power is applied:
Solutions :
a) Make sure "AEC-BOX-80 to VTR" cable is in place.
b) Make sure power to the VTR is ON.
c) Fix broken LED wiring.
d) Return AEC-BOX-80 for repairs.

Problem #2: Power LED blinks ON initially, then stays off:
Solutions :
a) Return AEC-BOX-80 for repairs.

Problem #3: Power LED blinks OFF during operations:
Solutions :
a) See the LED OPERATIONS section of this manual.
b) In the standalone mode, this is normal.
c) Make sure proper (Sony or AEC) mode is selected.
d) Make sure the controller's UART parameters (baud rate, parity, etc.) match those of the AEC-BOX-80.
e) Check cables for shorts, opens, crossed wires.
f) If using RS232, limit cable length to 30 meters.

Problem #4: Controller doesn't reliably receive messages:
Solutions :
a) The controller must be able to receive ALL bytes in a message without any OVERRUN errors, even if interrupts occur during reception. Change interrupt priorities, disable some, etc.

Problem #5: Some time code counts are missing:
Solutions :
a) This is normal at high tape shuttle speeds, where serial delays are longer than one frame.
b) SMPTE drop frame counting eliminates some counts.
c) Use a higher quality tape and/or VTR which does not have any dropouts, bit errors, etc..

7-BIT ASCII CODE CHART

Dec	Hex	Key	Char	Description	Dec	Hex	Char	Dec	Hex	Char
0	00h	^2	NUL	null char.	43	2B	+	86	56	V
1	01h	^A	SOH	start heading	44	2C	,	87	57	W
2	02h	^B	STX	start of text	45	2D	-	88	58	X
3	03h	^C	ETX	end of text	46	2E	.	89	59	Y
4	04h	^D	EOT	end of trans.	47	2F	/	90	5A	Z
5	05h	^E	ENQ	enquiry	48	30	0	91	5B	[
6	06h	^F	ACK	acknowledge	49	31	1	92	5C	\
7	07h	^G	BEL	ring bell	50	32	2	93	5D	]
8	08h	^H	BS	backspace	51	33	3	94	5E	^
9	09h	^I	HT	horiz. tab	52	34	4	95	5F	_
10	0Ah	^J	LF	line feed	53	35	5	96	60	`
11	0Bh	^K	VT	vertical tab	54	36	6	97	61	a
12	0Ch	^L	FF	form feed	55	37	7	98	62	b
13	0Dh	^M	CR	carriage ret.	56	38	8	99	63	c
14	0Eh	^N	SO	shift out	57	39	9	100	64	d
15	0Fh	^O	SI	shift in	58	3A	:	101	65	e
16	10h	^P	DLE	data link esc	59	3B	;	102	66	f
17	11h	^Q	DC1	device ctrl 1	60	3C	<	103	67	g
18	12h	^R	DC2	device ctrl 2	61	3D	=	104	68	h
19	13h	^S	DC3	device ctrl 3	62	3E	>	105	69	i
20	14h	^T	DC4	device ctrl 4	63	3F	?	106	6A	j
21	15h	^U	NAK	no acknwldge	64	40	@	107	6B	k
22	16h	^V	SYN	synch. idle	65	41	A	108	6C	l
23	17h	^W	ETB	end TX block	66	42	B	109	6D	m
24	18h	^X	CAN	cancel	67	43	C	110	6E	n
25	19h	^Y	EM	end of medium	68	44	D	111	6F	o
26	1Ah	^Z	SUB	substitute	69	45	E	112	70	p
27	1Bh	^[	ESC	escape	70	46	F	113	71	q
28	1Ch	^\	FS	file sepratr.	71	47	G	114	72	r
29	1Dh	^]	GS	group sep.	72	48	H	115	73	s
30	1Eh	^6	RS	record sep.	73	49	I	116	74	t
31	1Fh	^-	US	unit sepratr.	74	4A	J	117	75	u
32	20h	SPC		space	75	4B	K	118	76	v
33	21h	!	!	exclamation	76	4C	L	119	77	w
34	22h	"	"	double quote	77	4D	M	120	78	x
35	23h	#	#	number sign	78	4E	N	121	79	y
36	24h	$	$	dollar sign	79	4F	O	122	7A	z
37	25h	%	%	percent sign	80	50	P	123	7B	{
38	26h	&	&	ampersand	81	51	Q	124	7C	|
39	27h	'	'	apostrophe	82	52	R	125	7D	}
40	28h	(	(	left parenth	83	53	S	126	7E	~
41	29h	)	)	right parenth	84	54	T	127	7F	DEL
42	2Ah	*	*	asterisk	85	55	U			

ASCII is an abbreviation for
"the American Standard Code for Information Interchange".

NOTE: The keystrokes indicated above are for IBM PC's,
and may be slightly different for your equipment.

NUMBER SYSTEM CONVERSION TABLE

This chart will help you make conversions between the various numbering systems which are used in this manual.

Hexadecimal	(MSB) Binary (LSB)	Decimal	BCD
0	0 0 0 0	0	0
1	0 0 0 1	1	1
2	0 0 1 0	2	2
3	0 0 1 1	3	3
4	0 1 0 0	4	4
5	0 1 0 1	5	5
6	0 1 1 0	6	6
7	0 1 1 1	7	7
8	1 0 0 0	8	8
9	1 0 0 1	9	9
A	1 0 1 0	10	invalid
B	1 0 1 1	11	invalid
C	1 1 0 0	12	invalid
D	1 1 0 1	13	invalid
E	1 1 1 0	14	invalid
F	1 1 1 1	15	invalid
(base 16)	(base 2)	(base 10)	

(BCD is an abbreviation for "Binary Coded Decimal")

PACKED BCD NUMBERS

A "packed BCD" byte contains two BCD digits in an 8-bit byte. Bits 7-4 (upper nibble) contain the upper BCD digit, and bits 3-0 (lower nibble) contain the lower BCD digit.

For example, incrementing BINARY 09h leaves you with 0Ah, but incrementing PACKED BCD 09h leaves you with 10h. A packed BCD number such as 0Ah would be invalid, because "A" is not a valid BCD digit.

Here is one more example, showing the packed BCD format as used for time bits I/O. The 30 second (half minute) mark would be read (or written) as a 30h byte, even though 30 decimal is the same as binary 1Eh.

WHERE/HOW TO ORDER COPIES OF STANDARDS

We suggest that you fax, call, or write the organizations below for current prices and ordering/payment procedures. Due to copyright restrictions, we cannot provide standards copies for you. It takes some of these organizations up to 2 months to respond, so plan ahead. Also, please let us know if you find anything on this page which needs updating. Thanks.

SMPTE Engineering Standards Service
595 West Hartsdale Avenue
White Plains, NY 10607
U.S.A.
Tel: +1-914-761-1100 Fax: +1-914-761-3115

1)	SMPTE 207M-1992	ESbus Electrical/Mechanical	$16.00
2)	SMPTE RP113-1992	ESbus Supervisory Protocol	$16.00
3)	SMPTE RP138-1992	ESbus Control Message Architecture	$13.00
4)	SMPTE RP139-1992	ESbus Tributary Interconnection	$16.00
5)	SMPTE RP163-1992	ESbus System Service Messages	$16.00
6)	SMPTE RP170-1993	ESbus VTR-Specific Messages	$24.00
7)	SMPTE RP172-1993	ESbus Common Messages	$18.00
8)	SMPTE 12M-1986	Time and Control Code for Television	$16.00
9)	SMPTE 262M	Data Storage & Trans. - Binary Groups	$13.00
A)	SMPTE RP159-1991	VITC and LTC Relationship	$10.00
B)	SMPTE RP164-1992	Location of VITC	$10.00

European Broadcasting Union (EBU)
Technical Department
Case Postale 67
CH-1218 Grand-Saconnex/Geneve
SWITZERLAND
Tel: +41-22-717.21.11 Fax: +41-22-717.24.81
You must order the "Annual Volume of EBU Official Technical Texts",
which (for 250 Swiss Francs) includes the following:
1) N12 Time & Control Codes for Television
2) N18 Relationship Between Time Code and PAL 8-Field Sequence
3) I29 Recording of Information in User Bits

Telecommunications Industry Association (TIA)
(formerly part of Electronic Industries Association - EIA)
2500 Wilson Blvd.
Arlington, VA 22201
U.S.A.
Tel: +1-703-907-7700 Fax: +1-703-907-7727
These standards are sold only by Global Engineering Documents:
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1) TIA/EIA Standard RS232-E $49.00
2) TIA/EIA Standard RS422-A $51.00
3) TIA/EIA Standard RS485 $60.00